

phrases such as “wherein the step of writing the interlaced line to the second line buffer overlaps in time with the step of reading the second non-interlaced line from the second line buffer” have been added in order to more specifically and distinctively define the invention. Applicants submit that amended claims 16-18 now define the invention with sufficient particularity and distinctiveness and are adequately supported by the specification (e.g., by FIGS. 5-7 and the accompanying text). Therefore, Applicants respectfully submit that the rejection of claims 16-18 under 35 U.S.C. § 112, first paragraph, is traversed.

Claims 1-15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Donovan (5781241). This rejection is respectfully traversed.

Claim 1, which has been amended to more distinctly claim Applicants’ invention, recites a device for flicker filtering a plurality of non-interlaced lines containing graphics data to form a plurality of interlaced lines. The device is adapted for operation with two line buffers and includes:

- 1) a data packer having an input and two outputs for converting data from an external format to an internal format, the two outputs adapted to write data in the internal format to a first line buffer and to a second line buffer respectively; and
- 2) a data unpacker having two inputs and two outputs for converting data from the internal format to the external format, the two inputs adapted to receive data read from the first line buffer and from the second line buffer respectively, . . . [emphasis added]

The device further includes a filter circuit for filtering the data. As noted in the specification (see p. 9, ll. 5-9), the “internal format” is the format used in storing data to the line buffers; while the “external format” is the one used in processing data in the filter circuit. The data packer converts from the external to the internal format; while the data unpacker converts from the internal to the external format. In a preferred embodiment (see p. 9, ll. 10-12), the external format is the 4:4:4 signed YCrCb format; while the internal format may be either the 4:2:2 or the 4:1:1 YCrCb

format. Since the 4:2:2 and 4:1:1 formats are shorter than the 4:4:4 format, one advantage of this embodiment of the claimed feature is that smaller line buffers may be used, thus reducing the amount of silicon real estate required to implement the device. Alternately, if a certain amount of silicon real estate has been allocated to the device, since the claimed approach uses less real estate for the line buffers, more real estate may be used to implement other functionality such as more sophisticated filtering.

The cited art clearly does not show or suggest this claimed feature. Donovan also concerns a device for flicker filtering non-interlaced lines to produce interlaced lines and Donovan's device includes line memories and ALUs, which roughly correspond to the line buffers and filter circuit recited above. However, in all of Donovan's figures and explanations, Donovan does not show or suggest that different formats could be used to store data to the line memories and to process the data in the ALUs. For example, in Donovan's FIGS. 11 and 14, which are the only figures depicting line memories and ALUs, Donovan does not depict anything even remotely similar to the data packers and data unpackers recited above, nor does the accompanying text describe or suggest changing formats between the line memories and ALUs. Donovan simply states, as a representative example, that "the data from the line memory LM1 (L2) is read, scaled by the factor A1, and added in the ALU1 to the incoming line (L3) scaled by A2. This sum ($A1*L2 + A2*L3$) is then written back into the line memory LM1 . . ." (col. 6, ll. 28-30). Clearly, there is no suggestion of changing formats between the line memory and the ALU. Applicants teach and claim changing formats, but Applicants' teaching cannot be used as the basis for rejection.

In his remarks, the Examiner contends that Donovan's scaling function implies the existence of a data packer - in other words, that Donovan's scaling operation is equivalent to

changing formats. Applicants respectfully traverse this characterization. Donovan's scaling function refers to vertical scaling between the incoming noninterlaced lines and the outgoing interlaced lines. In Donovan's example, if the scaling ratio is 1:1 (i.e., no scaling), then each outgoing TV line is produced from two incoming VGA lines. A scaling ratio of 7/8 means that 7 TV lines are generated from every 16 VGA lines. This affects the coefficients A_1, A_2, \dots used in the ALU for forming the TV lines, but scaling does not imply anything about the format used by the line memories, let alone whether it is different from the format used in the ALUs. Hence, scaling also does not imply the existence of a data packer or data unpacker.

To continue Donovan's 7/8 scaling example, TV line 5 is formed from VGA lines 7, 8, 9, and 10 according to the expression: $A_1 * L_7 + A_2 * L_8 + A_2 * L_9 + A_3 * L_{10}$ (col. 6, ll. 63-65). This expression is a result of scaling. However, the expression does not imply anything about the format used to store the VGA lines (or intermediate sums or the final expression) in the line memory. To wit, if the ALU processes the VGA lines using one format, such as 4:4:4 YCrCb format, the fact that TV line 5 is generated using the above equation does not imply that the intermediate or final results are stored in the line memory using a different format, such as 4:1:1 YCrCb format.

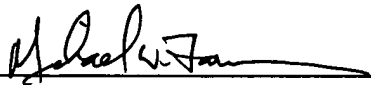
For the foregoing reasons, Applicants respectfully submit that claim 1 and its dependent claims 2-11 are patentably distinctive from Donovan. Furthermore, independent claims 12 and 15-18 include limitations similar to those in claim 1. Hence, for the same reasons given above with respect to claim 1, Applicants respectfully submit that Donovan also does not teach or suggest claims 12 and 15-18 and their dependent claims.

Hence, reconsideration and allowance of claims 1-18 as amended are solicited.

Respectfully submitted,

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